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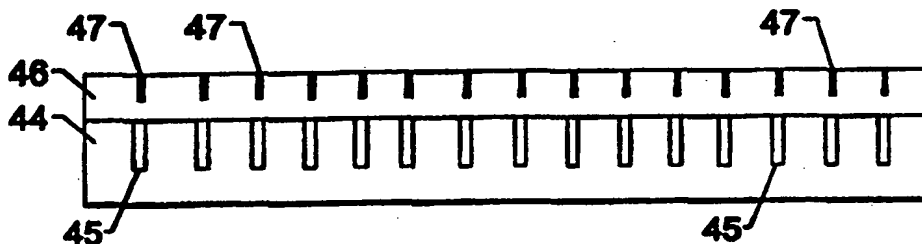




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(54) Title: GROUP III NITRIDE PHOTONIC DEVICES ON SILICON CARBIDE SUBSTRATES WITH CONDUCTIVE BUFFER INTERLAYER STRUCTURE



## (57) Abstract

An optoelectronic device with a Group III nitride active layer is disclosed that comprises a silicon carbide substrate; an optoelectronic diode with a Group III nitride active layer; a buffer structure selected from the group consisting of gallium nitride and indium gallium nitride between the silicon carbide substrate and the optoelectronic diode; and a stress-absorbing structure comprising a plurality of predetermined stress-relieving areas within the crystal structure of the buffer structure, so that stress-induced cracking that occurs in the buffer structure occurs at predetermined areas rather than elsewhere in the buffer structure.



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## **Group III Nitride Photonic Devices on Silicon Carbide Substrates with Conductive Buffer Interlayer Structure**

### **Field of the Invention**

5           This invention relates to photonic devices in wide bandgap materials, and in particular relates to photonic devices formed with Group III nitride active layers on silicon carbide substrates.

### **Background of the Invention**

10           The semiconductor materials with wide bandgaps such as diamond, silicon carbide, and gallium nitride have become of significant interest in recent years because their wide bandgap characteristics provide them with the capability to emit light of higher energy (with correspondingly higher frequency and shorter wavelength) than do other semiconductor materials such as silicon or gallium arsenide. In particular, silicon carbide, gallium nitride, and certain other Group III  
15           nitrides have bandgaps large enough to produce visible light throughout the visible spectrum, including the higher-energy blue portion. They thus provide the basis for semiconductor lasers and light emitting diodes (LEDs) with blue and green emissions.

          Of these materials, gallium nitride is of particular interest because it is a direct semiconductor, *i.e.*, the transition from the valence band to the conduction band does  
20           not require a change in crystal momentum for the electron. As a result, the transition produces light very efficiently. In contrast silicon carbide is an indirect semiconductor; the bandgap transition energy is given off partly as a photon and partly as vibrational energy. Thus, gallium nitride offers the advantage that for a given operating voltage and current, it will produce light more efficiently than silicon  
25           carbide

          As with other semiconductor materials, however, the first step in forming a workable photonic device is to build-up or otherwise obtain a suitable crystal structure with the desired active layer. Because of the differences in the structural characteristics of semiconductor materials, however, particularly their crystal lattice  
30           structures, the materials which will workably support Group III nitride active layer devices are somewhat limited.

          Presently, commercially available structures for a light emitting diode photonic device are formed of a gallium nitride or related Group III nitride active



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layer on a sapphire substrate. Sapphire ( $\text{Al}_2\text{O}_3$ ) provides a relatively close lattice match to Group III nitrides, but also suffers certain disadvantages, the most limiting of which is its electrically insulating character. Thus, when Group III nitride active and buffer layers (*i.e.*, the intermediate layers that provide a crystal structure transition from the substrate to the active layer) are built on sapphire, the sapphire cannot be used as a conductive pathway to the active portions of the device. This limits the type of devices that can be designed and produced on sapphire, and in particular limits the ability to form "vertical" devices in which the device contacts can be placed on opposite surfaces of the device with a direct conductive path through the substrate, buffers, and active layer. and the other contacts on the opposite of the device.

Accordingly, interest, including that of the assignee of the present invention, has focused upon the use of other materials as substrate candidates for Group III nitride photonic devices. Silicon carbide ( $\text{SiC}$ ) is a particularly attractive candidate because it can be made conductive, has a lattice match that can be appropriately buffered to a Group III nitride active layer, and has excellent thermal and mechanical stability.

Nevertheless, silicon carbide's crystal lattice structure is such that some of the best candidates for an appropriate Group III buffer layer on a silicon carbide substrate are insulating rather than conductive. Thus, although the silicon carbide substrate can be made conductive, some of the preferred buffer layers between silicon carbide substrates and Group III active layer photonic devices remain insulating, thus minimizing the advantages of the conductive silicon carbide substrate.

For example, aluminum nitride ( $\text{AlN}$ ) provides an excellent buffer between a silicon carbide substrate and a Group III active layer, particularly a gallium nitride active layer. Aluminum nitride is, however, insulating rather than conductive. Thus, structures with aluminum nitride buffer layers require shorting contacts that bypass the aluminum nitride buffer to electrically link the conductive silicon carbide substrate to the Group III nitride active layer. As noted above such shorting contacts preclude some of the more advantageous device designs.

Alternatively, conductive buffer layer materials such as gallium nitride ( $\text{GaN}$ ), aluminum gallium nitride ( $\text{AlGaN}$ ), or combinations of gallium nitride and aluminum



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gallium nitride can eliminate the shorting contacts. In turn, eliminating the shorting contact reduces the epitaxial layer thickness, decreases the number of fabrication steps required to produce devices, reduces the overall chip size, and increases the device efficiency. Accordingly, Group III nitride devices can be produced at lower cost with  
5 a higher performance.

Nevertheless, although these conductive buffer materials offer these advantages, their crystal lattice match with silicon carbide is less satisfactory than is that of aluminum nitride. Accordingly, when epitaxial buffer layers of gallium nitride, aluminum gallium nitride, or combinations thereof are grown on silicon  
10 carbide substrates, they tend to produce excessive cracking in subsequent epilayers that are required for photonic devices such as light-emitting diodes or laser diodes.

Thus, there exists a need for a buffer structure that offers the crystal lattice match advantages of aluminum nitride and yet which at the same time offers the conductivity advantages of gallium nitride or aluminum gallium nitride and that can  
15 be used in conjunction with conductive silicon carbide substrates rather than insulating sapphire substrates.

#### Object and Summary of the Invention

Therefore, it is an object of the present invention to produce photonic devices and their wafer precursors, with a Group III nitride active layer, a conductive silicon  
20 carbide substrate, and a conductive buffer layer, but that avoids the cracking and other problems that have to date hindered such combinations of materials and layers.

The invention meets this object with a photonic device with a Group III nitride active layer which comprises a silicon carbide substrate, an optoelectronic diode with a Group III nitride active layer, and a buffer structure between the silicon carbide  
25 substrate and the optoelectronic diode in which the buffer structure is both conductive and which provides the appropriate crystalline properties.

In one aspect, the buffer structure is selected from the Group consisting of gallium nitride and indium gallium nitride (InGaN), and incorporates a stress absorbing structure comprising a plurality of predetermined stress relieving areas  
30 within the crystal structure of the buffer layer so that stress induced cracking that occurs in the buffer occurs at the predetermined areas rather than elsewhere in the buffer.



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In another aspect, the buffer layer includes a plurality of discrete crystal portions selected from the group consisting of gallium nitride and indium gallium nitride on the surface of the silicon carbide substrate for minimizing or eliminating the heterobarrier between silicon carbide and aluminum gallium nitride buffer structure.

5       The foregoing, and other objects and advantages of the invention, and the manner of accomplishing the same will become clearer when taken in conjunction with the accompanying detailed description and drawings in which:

Brief Description of the Drawings

10       Figure 1 is a cross-sectional view of a prior-art diode with a shorting ring contact;

      Figure 2 is a cross-sectional view of a vertical diode that can be produced to the present invention;

      Figure 3 is an enlarged schematic view of a pixel formed according to the present invention;

15       Figure 4 is a schematic view of a display that includes a plurality of pixels that incorporates structures according to the present invention;

      Figure 5 is a schematic view of a silicon carbide wafer that incorporates the stress relieving structure according to the present invention;

      Figure 6 is a cross-sectional view of the wafer of Figure 5;

20       Figure 7 is a cross-sectional view of the wafer of Figure 5 and showing in schematic view a buffer layer grown thereon;

      Figure 8 is a cross-sectional view of a wafer incorporating second embodiment of the invention;

25       Figure 9 is a cross-sectional view identical to Figure 8 but showing additional crystal growth thereon;

      Figure 10 is a 10X magnification photo from a scanning electron microscope (SEM) of an epilayer that does not incorporate the present invention;

      Figure 11 is an 10X SEM photo showing an epilayer according to the present invention;

30       Figure 12 is another 10X SEM photo showing an epilayer according to the present invention;

      Figure 13 is a 50X SEM photo of an epilayer similar to Figure 12;



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Figure 14 is a 100X SEM photo of an epilayer according to the present invention;

Figure 15 is another 100X SEM photo showing another epilayer that does not incorporate the present invention;

5        Figures 16, is a 15,000X SEM photo of a second embodiment of the invention; and

Figure 17 is a 50,000X SEM photo of the second embodiment.

#### Detailed Description

Figure 1 is a cross-sectional view of a prior art device that is broadly  
10        designated at 20. As illustrated in Figure 1, the device 20 includes a silicon carbide substrate 21, a contact 22 to the "back" of the substrate 21, a Group III nitride active layer 23, a buffer layer 24 which is insulating rather than conductive, shorting contacts 25 for providing electrical contact between the conductive silicon buffer 21 and the active layer 23, and a top contact 26 for completing the circuit and permitting  
15        current to flow through the device in operation.

Figure 2 shows the manner in which the present invention provides for a more compact device. In Figure 2 the device is broadly designated at 30, and includes a conductive silicon carbide substrate 31, a back contact 32, an active layer 33 and a conductive buffer structure 34, along with a top contact 35. The invention thus  
20        eliminates the shorting contacts (typically shorting ring contacts) 25 of the device of Figure 1. As a result, the device 30 is easier to manufacture and more efficient in operation. It will be understood that the active layer 33 as discussed herein can represent a device with a single p-n junction, a single or double p-n heterojunction or a p-n junction quantum well structure. Such structures are described in a number of  
25        prior U.S. patents including Nos. 5,393,993 and 5,592,501, and will not be otherwise discussed in detail herein other than to further illustrate the present invention.

Figure 3 illustrates that the device 30 according to the present invention can be incorporated with similar devices of different emitting wavelengths, in particular a red emitting diode 36 and a green emitting diode 37, as part of a three-color pixel broadly  
30        designated at 40 which in turn can be one of a plurality of such pixels in a display 41. The vertical 42 and horizontal 43 lines shown schematically in Figure 4 represent the



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rows and columns of pixels typically used in displays that incorporate light emitting diodes.

In its first aspect, the invention is a photonic device with a Group III nitride active layer that comprises a silicon carbide substrate 31, a photonic diode with a Group III nitride active layer 33, and a buffer structure 34 selected from the group consisting of gallium nitride and indium gallium nitride between the silicon carbide substrate 31 and the diode 33. In particular, the buffer structure includes a stress absorbing structure that is made up of a plurality of predetermined stress relieving areas within the crystal structure of the buffer structure 34 so that stress induced cracking that occurs in the buffer structure occurs at the predetermined areas rather than elsewhere in the structure.

Figure 5 is a schematic view of a wafer that incorporates a plurality of device precursors and that incorporates the stress absorbing structure of the present invention. Figure 5 illustrates a wafer broadly designated at 44 on which is superimposed a grid pattern of grooves 45. Figure 6 shows the same wafer 44 and grooves 45 in a cross-sectional orientation. When the next epitaxial layer 46 (Figure 7) is grown on the wafer 44 with its grooves 45, the surface of the epitaxial layer 46 tends to have a series of discontinuities 47 whose positions reflect the positions of the grooves 45 that form the pattern in the wafer 44. These discontinuities 47 form areas at which stress will relieve itself as the crystal lattice structure of the buffer layer 46 grows on the silicon carbide wafer 44. As a result, such stress resulting from lattice mismatches (or other factors) occurs at intended rather than random positions, thus permitting devices to be formed in the remaining areas without significant risk of stress cracking.

As noted above and illustrated in Figure 5, in one preferred embodiment the predetermined pattern of stress relieving areas comprises a grid and the grid can preferably be formed in any desired or necessary size that defines individual devices. For example, where the individual devices will be light emitting diodes, a preferable grid pattern defines squares of about 250 microns per side. Alternatively, for different devices such as laser diodes, the grid can define rectangles of about 250 by 500 microns ( $\mu$ ).



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Figure 10 is a SEM photograph taken at a 10X magnification (10 times actual size) that shows the extent to which cracking—seen as the somewhat triangular or hexagonal patterns—can mar an epitaxial layer and render it defective or useless for photonic devices.

5        Figure 11 is another 10X SEM photograph and illustrates a grid pattern of grooves in the epitaxial layer. In comparison with Figure 10, the surface shown in Figure 11 is relatively free of cracking defects.

Figure 12 is another 10X SEM photograph, and illustrates a smaller grid pattern. As with Figure 11, it is quite free of the cracks illustrated in Figure 10.

10        Figure 13 is a 50X SEM photograph that particularly illustrates the advantages of the invention. In Figure 13, one of the grid sections contains a large defect (in a somewhat "X" shape). The defect ends, however, at the grid line and spoils only one device (or device precursor) rather than a multi-device portion of the wafer.

Figure 14 is a 100X SEM photograph that similarly illustrates one defective grid portion (in the lower right portion of the photograph) for which the defect ends at the grid line rather than propagating further throughout the surface.

Figure 15 is a 100X SEM photograph that again illustrates a surface that does not incorporate any of the embodiments of the present invention. As with Figure 10, the geometric pattern of defects is quite evident.

20        In another embodiment, the stress absorbing structure can comprise a predetermined pattern of small mesa structures that are best illustrated in Figures 8 and 9. In Figures 8 and 9 the silicon carbide substrate is designated at 50 and the small mesa structures at 51. The mesa structures 51 are formed of a material upon which the growth of the selected buffer material is disfavored. For a gallium nitride or indium gallium nitride buffer structure, the preferred materials are selected from the group consisting of silicon dioxide, silicon nitride, and aluminum oxide.

Figure 9 illustrates the same structure as Figure 8, but with the buffer material grown as an epitaxial layer on the silicon carbide substrate 50. The epitaxial layer portions are illustrated at 52. As Figure 9 illustrates, because growth of the buffer material is disfavored on the mesas 51, the epitaxial layer 52 forms a pattern which again exhibits predetermined stress-relieving discontinuity structures therebetween. As in the previous embodiment, the areas between the mesas can be tailored to be

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about the same size as the individual device, which, as noted above, is on the order of about 250 microns for LEDs and about 250 x 500 $\mu$  for laser diodes. It will be understood, however, that the particular size of the pattern of either the grids or the mesa structures is illustrative rather than limiting of the present invention.

5 It will be understood that although the wafer structures according to the invention are particularly advantageous for optoelectronic devices, they are not limited to such, and the superior structural properties are advantageous for other devices formed upon the wafers.

As noted in the background portion, the optoelectronic device formed upon the buffer layer, and as typically illustrated at 23 in Figure 1 and 33 in Figure 2, is  
10 generally not a single layer, but rather is a multi-layer diode selected from the group consisting of p-n homojunctions, p-n heterojunctions, p-n single and double heterojunctions, and p-n junction quantum well structures.

In preferred embodiments, the silicon carbide substrate has a polytype selected  
15 from the group consisting of the 3C, 4H, 6H, and 15R polytypes. In the most preferred embodiments, the Group III nitride active layer of the diode comprises gallium nitride or indium gallium nitride.

Figures 16 through 18 illustrate another embodiment of the invention. In general, in schematic fashion, the overall structure is again illustrated by Figure 2 and  
20 comprises the silicon carbide substrate 31, the photonic diode 33 and the buffer layer 34. In this embodiment, however, the buffer layer is aluminum gallium nitride rather than gallium nitride or indium gallium nitride. This embodiment includes a plurality of discrete crystal portions that appear as the white colored dots in Figure 16-18. The discrete crystal portions are selected from the group of gallium nitride and indium  
25 gallium nitride and are on the surface of the silicon carbide substrate for minimizing or eliminating the heterobarrier between the silicon carbide substrate 31 and the aluminum gallium nitride buffer structure 34.

In preferred embodiments, the discrete crystal portions are present in an amount sufficient to minimize or eliminate the heterobarrier but less than the amount  
30 that would detrimentally affect or destroy the function of any resulting diode device built on the silicon carbide substrate 31. As illustrated in the photographs of Figures



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16-18 the discrete crystal portions are present in an amount of between about 40 and 60 per square micron.

Additionally, the sizes of the discrete crystal portions are preferably large enough to minimize or eliminate the heterobarrier, but smaller than a size that would detrimentally affect or destroy the function of any resulting diode device built on the silicon carbide substrate 31. In preferred embodiments, the discrete crystal portions are between 0.01 and 0.1 microns in diameter.

As in the previous embodiments, the optoelectronic device 33 formed on the buffer structure can comprise a light emitting diode or laser diode, and the resulting light emitting diode can be incorporated into pixels which in turn can be incorporated into displays.

In preferred embodiments, the aluminum gallium nitride buffer layer has an atomic fraction of aluminum of between about 10 and 15%.

In another aspect, the invention comprises the method of producing the Group III nitride optoelectronic device on a silicon carbide substrate with a conductive buffer structure. In its method aspects, the invention comprises forming a structural pattern on the surface of a silicon carbide substrate that has otherwise been prepared for crystal growth thereon; forming a buffer layer selected from the group consisting of gallium nitride and indium gallium nitride on the patterned surface of the silicon carbide substrate so that the buffer layer exhibits features that follow the pattern of openings in the surface of the silicon carbide substrate; and thereafter forming a optoelectronic device with a Group III nitride active layer on the buffer layer.

As described with respect to the structural aspects, the step of forming the structural pattern can comprise forming a pattern of openings in the surface of the silicon carbide substrate or forming a pattern of mesa structures on the surface of the silicon carbide substrate.

When the pattern is formed of openings, the step of forming the openings can comprise techniques such as reactive ion etching or masking and etching steps. Each of these steps is relatively well understood for silicon carbide and will not be otherwise described except to note, for example, U.S. Patents Nos. 4,865,685 and 4,981,551 describe exemplary dry etching procedures for silicon carbide.



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Where the mesa structures are incorporated, they are preferably selected from the group consisting of silicon dioxide, silicon nitride, and aluminum oxide. As in the structural environments, the optoelectronic device with the Group III active layer is preferably formed of gallium nitride or indium gallium nitride.

5       As in the structural embodiments, the method of the invention can comprise forming a light emitting diode or a laser diode, and when a light emitting is formed, the method can further comprise incorporating the LED into a pixel, and the pixel into a display.

10       In an alternative method aspect, the buffer structure of the invention structure is formed of aluminum gallium nitride on a silicon carbide substrate that has been previously prepared by forming a plurality of discrete crystal portions selected from the group consisting of gallium nitride and indium gallium nitride on the silicon carbide surface. Thereafter, the optoelectronic device with the Group III nitride active layer is formed on the buffer layer.

15       As set forth in the structural aspects of the invention, the method comprises forming discrete crystal portions of a size and in an amount that is sufficient to minimize or eliminate the heterobarrier, but less than sizes or amounts that would detrimentally affect or destroy the function of any resulting diode device built on the silicon carbide substrate. In particular the invention provides a robust structure that  
20       can withstand normally expected levels of electrostatic discharge.

In the second method aspect, the resulting device can be formed as a light emitting diode so that the method can further comprise incorporating the LED pixel and the pixel into a display. The method can alternatively comprise forming a laser diode rather than an LED.

25       As in the other aspects of the invention, when the aluminum gallium nitride buffer layer is used, it is preferably has an atomic fraction of aluminum of between about 10 and 15%.

#### EXAMPLE

30       In a current process for producing conductive buffer LEDs and Laser Diodes, GaN dots are first deposited. The purpose of the GaN dots is to decrease the barrier between the SiC substrate and the Si-doped AlGaN buffer layer. This is done at considerably lower temperatures than are used for the other epitaxial layers in the



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structure. The size and density of the dots are shown in Figures 16 and 17. It is important to keep the dots relatively small so the electrostatic discharge will not be adversely affected. The GaN dots are deposited in about 6 seconds, and then "capped" with Si-doped  $\text{Al}_{.10}\text{Ga}_{.90}\text{N}$  for about 15 seconds. The purpose of this cap is to prevent the dissociation of the GaN dots upon heating. In this material system, adding any Al to GaN, *i.e.*,  $\text{Al}_{(1-x)}\text{Ga}_x\text{N}$  decreases the dissociation rate of the material because AlGa<sub>x</sub>N is more stable than GaN in an  $\text{NH}_3/\text{H}_2$  atmosphere. After the capping of the dots, the temperature is then ramped up to the buffer layer temperature. Temperatures are allowed to stabilize for 2 minutes after the ramp before commencing buffer layer growth.

In a specific run, a SiC wafer is heated in an atmosphere of  $\text{NH}_3$  and  $\text{H}_2$ , at 13 SLM and 15 SLM, respectively. These flows remain constant throughout the growth of the GaN dots, the AlGa<sub>x</sub>N cap, and the subsequent buffer layer. The temperature ramps up over the course of 10 minutes until the GaN dot temperature is reached which is about 960°C. After allowing the temperature in the system to stabilize for approximately 5 minutes, the dots are deposited by flowing 10–15cc of trimethyl gallium (TMG; -5°C, 600 torr) for about 6 seconds. In order to ensure that the dots are conducting,  $\text{SiH}_4$  is also added with the TMG flow. The amount of  $\text{SiH}_4$  is determined by growing a bulk GaN layer with a carrier concentration of about  $1 \times 10^{18} \text{ cm}^{-3}$ . Immediately following the deposition of the GaN dots, the TMG and  $\text{SiH}_4$  continue to flow, but now with the addition of trimethyl aluminum (TMA, 92cc, 25°C, 600 torr). This leads to a "cap" of about 10-11% AlGa<sub>x</sub>N. The growth time of the cap is 15 seconds. The flows (TMG, TMA, and  $\text{SiH}_4$ ) are then terminated and the temperature is ramped to the buffer temperature which is typically around 1060°C. The temperature ramp is 1 minute and is followed by a 2 minute period during which the temperature is allowed to stabilize. The buffer layer is then grown. Typical conditions are 18cc TMG/110ccTMA/.087cc  $\text{SiH}_4$ . Buffer layers consist of approximately 11-12% AlGa<sub>x</sub>N and are typically between about 1600 and 2700 Å thick.

In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they



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have been used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.



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**CLAIMS:**

1. An optoelectronic device with a Group III Nitride active layer, said device comprising:
  - a silicon carbide substrate;
  - 5 an optoelectronic diode with a Group III nitride active layer;
  - a buffer structure selected from the group consisting of gallium nitride and indium gallium nitride between said silicon carbide substrate and said optoelectronic diode; and
  - a stress-absorbing structure comprising a plurality of predetermined stress-relieving areas within the crystal structure of said buffer structure, so that stress-induced cracking that occurs in said buffer structure occurs at said predetermined areas rather than elsewhere in said buffer structure.
- 15 2. An optoelectronic device according to Claim 1 wherein said buffer structure is conductive
- 20 3. An optoelectronic device according to Claim 1 wherein said stress absorbing structure comprises a predetermined pattern of grooves in the surface of said silicon carbide substrate.
- 25 4. An optoelectronic device according to Claim 3 wherein said predetermined pattern is selected from the group consisting of a grid that defines squares of about 250 microns per side; and a grid that defines rectangles of about 250 by 500 microns.
- 30 5. An optoelectronic device according to Claim 1 wherein said stress absorbing structure comprises a predetermined pattern of small mesa structures formed of a material selected from the group consisting of silicon dioxide (SiO<sub>2</sub>), silicon nitride, and aluminum oxide.
6. An optoelectronic device according to Claim 1 wherein said diode is selected from the group consisting of p-n homojunctions, p-n single and double



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heterojunctions, and p-n quantum junction well structures, and said silicon carbide substrate has a polytype selected from the group consisting of the 3C, 4H, 6H, and 15R polytypes.

5           7.       An optoelectronic device according to Claim 1 wherein said Group III nitride active layer is selected from the group consisting of gallium nitride and indium gallium nitride.

10           8.       An optoelectronic device with Group III Nitride active layer, said device comprising:  
            a silicon carbide substrate;  
            an optoelectronic diode with a Group III nitride active layer;  
            an aluminum gallium nitride buffer layer between said silicon carbide substrate and said optoelectronic diode; and  
15           a plurality of discrete crystal portions selected from the group consisting of gallium nitride and indium gallium nitride on the surface of said silicon carbide substrate for minimizing or eliminating the heterobarrier between said silicon carbide substrate and said aluminum gallium nitride buffer structure.

20           9.       An optoelectronic device according to Claim 8 wherein said discrete crystal portions are present in an amount sufficient to minimize or eliminate the heterobarrier, but less than the amount that would detrimentally affect or destroy the function of any resulting diode device built on said silicon carbide substrate.

25           10.      An optoelectronic device according to Claim 8 wherein the sizes of said discrete crystal portions are large enough to minimize or eliminate the heterobarrier, but smaller than a size that would detrimentally affect or destroy the function of any resulting diode device built on said silicon carbide substrate.

30           11.      An optoelectronic device according to Claim 8 wherein the amount and size of said discrete crystal portions are sufficient to withstand normally expected levels of electrostatic discharge.



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12. An optoelectronic device according to Claim 1 or Claim 8 comprising a light emitting diode.

5 13. A pixel that incorporates a light emitting diode according to Claim 12.

14. A display that incorporates a plurality of pixels according to Claim 13.

10 15. An optoelectronic device according to Claim 1 or Claim 8 comprising a laser diode.

16. An optoelectronic device according to Claim 8 wherein said aluminum gallium nitride buffer layer has an atomic fraction of aluminum of between about 10 and 15 percent.

15

17. A method of producing a Group III nitride optoelectronic device on a silicon carbide substrate comprising:

forming a structural pattern on the surface of a silicon carbide substrate that has otherwise been prepared for crystal growth thereon;

20 forming a buffer layer selected from the group consisting of gallium nitride and indium gallium nitride on the patterned surface of the silicon carbide substrate so that the buffer layer exhibits features that follow the pattern in the surface of the silicon carbide substrate; and

25 forming an optoelectronic device with a Group III nitride active layer on the buffer layer.

18. A method according to Claim 17 wherein the step of forming the structural pattern comprises forming a pattern of openings in the surface of the silicon carbide substrate by masking the surface of the silicon carbide substrate and thereafter  
30 etching the masked surface to produce the structural pattern.



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19. A method according to Claim 17 wherein the step of forming the structural pattern comprises forming a pattern of mesa structures on the surface of the silicon carbide substrate from a material selected from the group consisting of silicon dioxide, silicon nitride, and aluminum oxide.

5

20. A method according to Claim 17 wherein the step of forming an optoelectronic device with a Group III nitride active layer comprises forming a device with an active layer selected from the group consisting of gallium nitride and indium gallium nitride.

10

21. A method of producing a Group III nitride optoelectronic device on a silicon carbide substrate comprising:

forming a plurality of discrete crystal portions selected from the group consisting of gallium nitride and indium gallium nitride on the surface of a silicon carbide substrate;

15

forming an aluminum gallium nitride buffer on the surface of the silicon carbide substrate with the discrete crystal portions, and wherein the discrete crystal portions minimize or eliminate the heterobarrier between the silicon carbide substrate and the aluminum gallium nitride buffer layer; and

forming an optoelectronic device with a Group III nitride active layer on the buffer layer.

20

22. A method according to Claim 21 wherein the step of forming the discrete crystal portions comprises forming the discrete crystal portions in an amount sufficient to minimize or eliminate the heterobarrier, but less than an amount that would detrimentally affect or destroy the function of any resulting diode device built on the silicon carbide substrate.

25

23. A method according to Claim 21 wherein the step of forming the discrete crystal portions comprises forming the portions with a size large enough to minimize or eliminate the heterobarrier, but smaller than a size that would

30



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detrimentally affect or destroy the function of any resulting diode device built on the silicon carbide substrate.

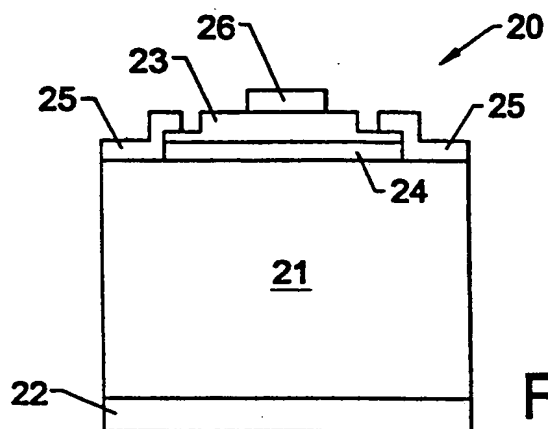
24. A method according to Claim 21 comprising forming the discrete  
5 crystal portions with sizes and in an amount sufficient for a resulting diode device to withstand normally expected levels of electrostatic discharge.

25. A wafer precursor for Group III nitride devices according to Claim 1,  
said precursor wafer comprising:  
10 a silicon carbide substrate wafer;  
a buffer layer on said substrate and selected from the group consisting of gallium nitride and indium gallium nitride; and  
a stress-absorbing structure comprising a plurality of predetermined stress-relieving areas within the crystal structure of said buffer layer, so that stress-induced  
15 cracking that occurs in said buffer layer occurs at said predetermined areas rather than elsewhere in said buffer structure.

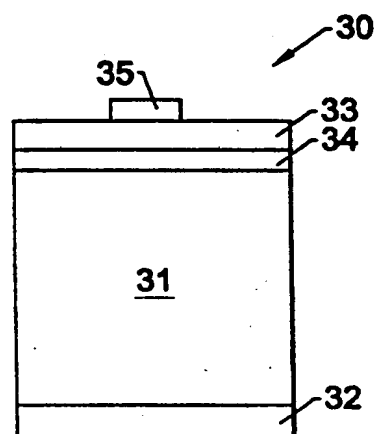
26. A wafer precursor for Group III nitride devices according to Claim 8,  
said wafer precursor comprising:  
20 a silicon carbide substrate wafer;  
an aluminum gallium nitride buffer layer on said silicon carbide substrate; and  
a plurality of discrete crystal portions selected from the group consisting of gallium nitride and indium gallium nitride on the surface of said silicon carbide  
substrate for minimizing or eliminating the heterobarrier between said silicon carbide  
25 substrate and said aluminum gallium nitride buffer layer.



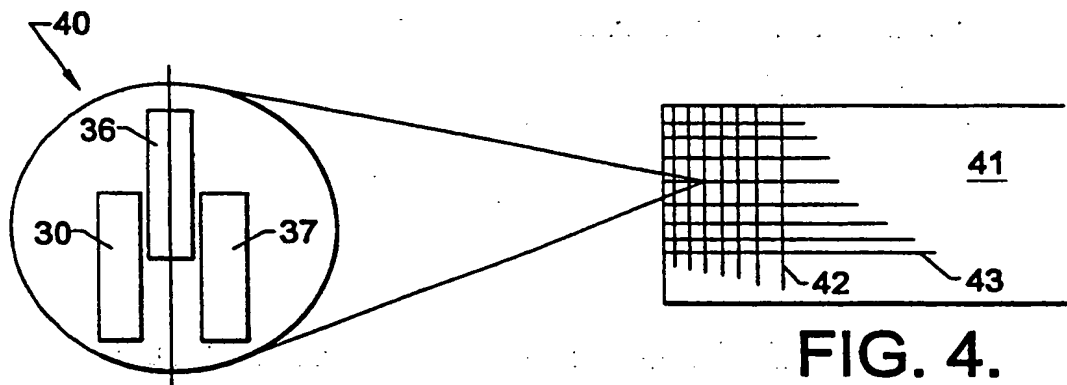
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**FIG. 1.**  
(PRIOR ART)



**FIG. 2.**

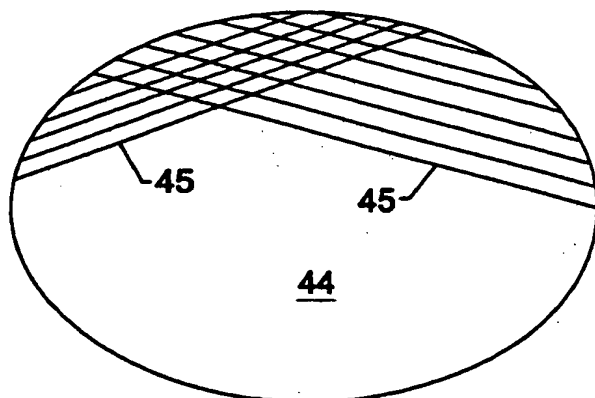


**FIG. 3.**

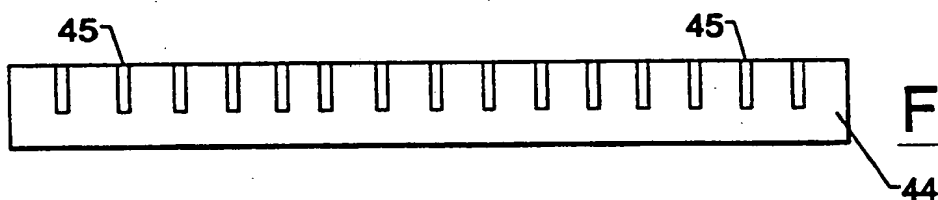
**FIG. 4.**



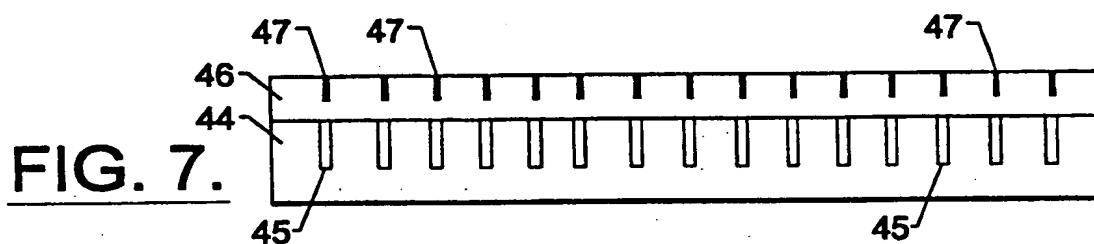
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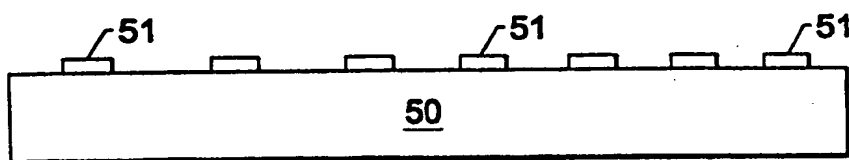
**FIG. 5.**



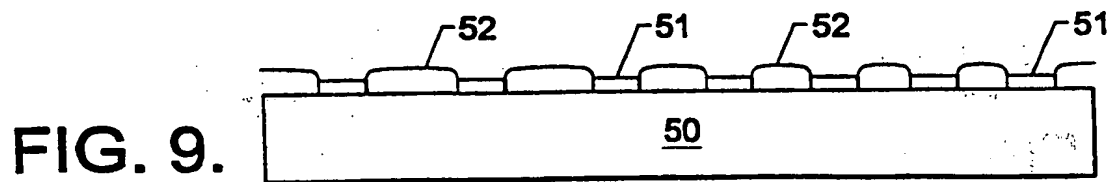
**FIG. 6.**



**FIG. 7.**



**FIG. 8.**



**FIG. 9.**





FIG. 10.



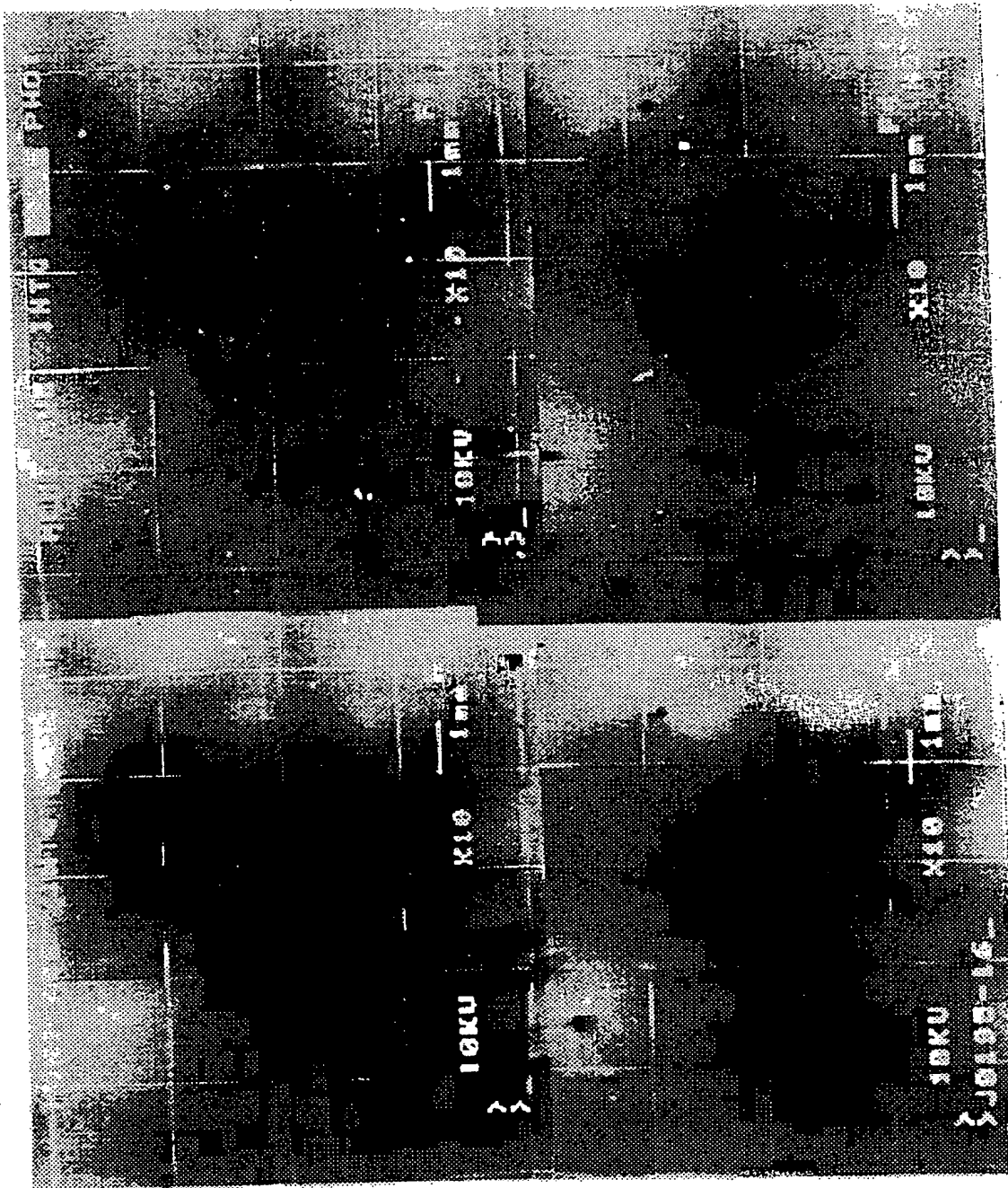


FIG. 11



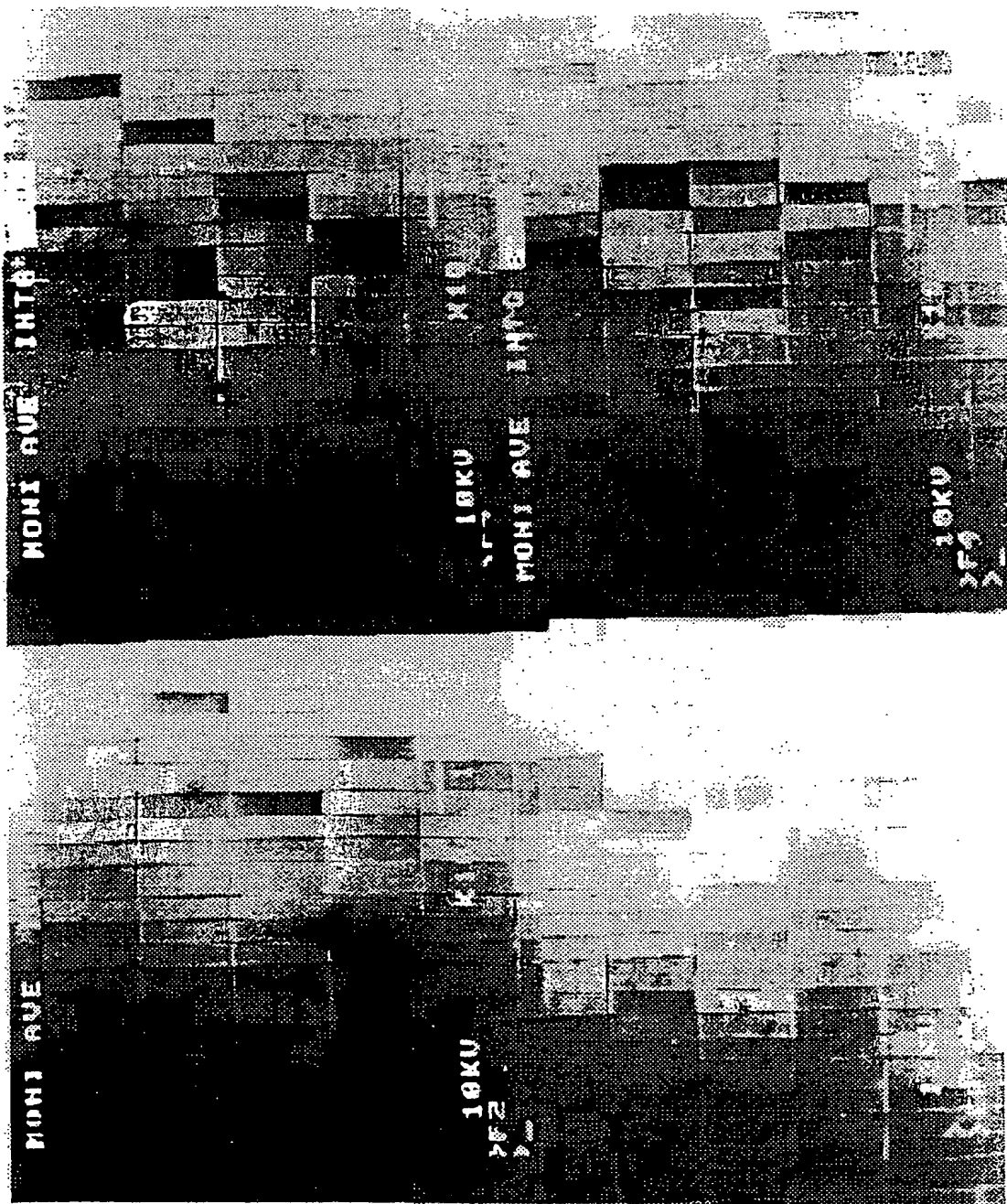


FIG. 12.



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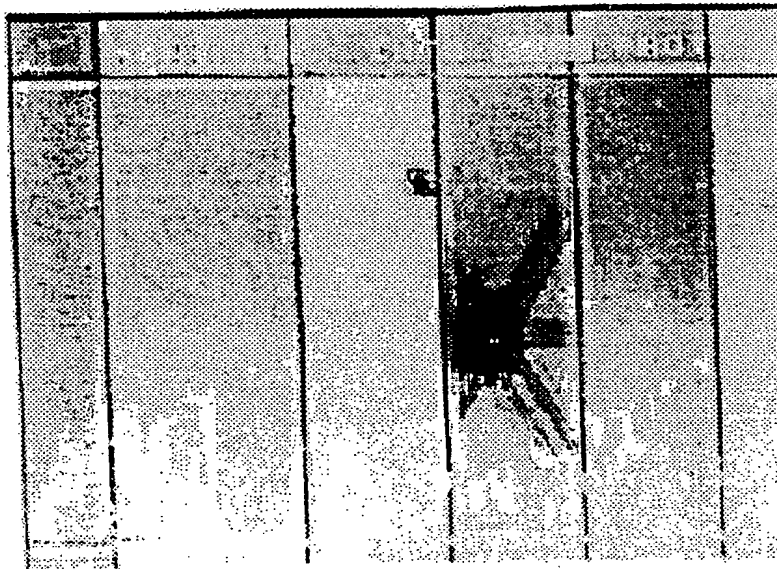


FIG. 13.

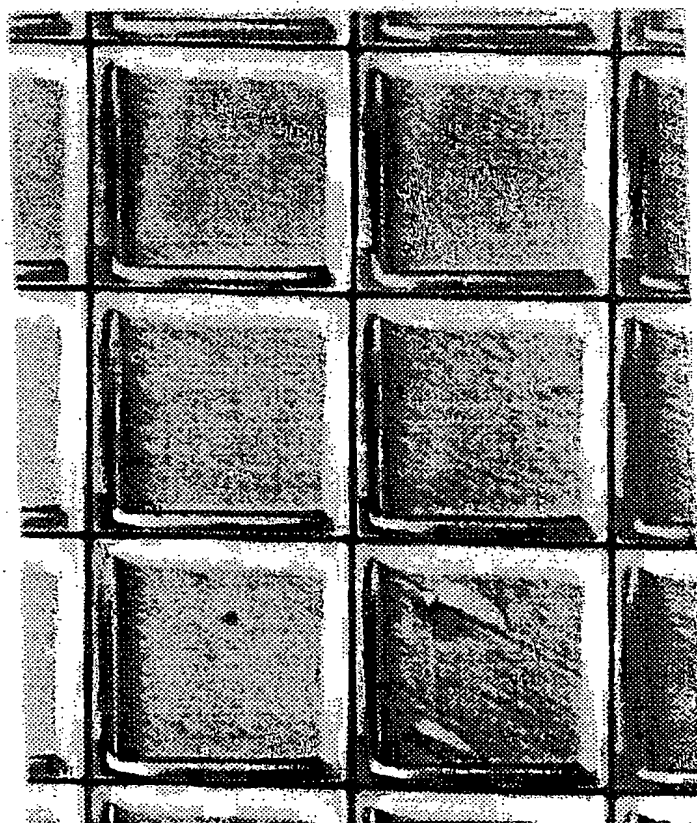


FIG. 14.



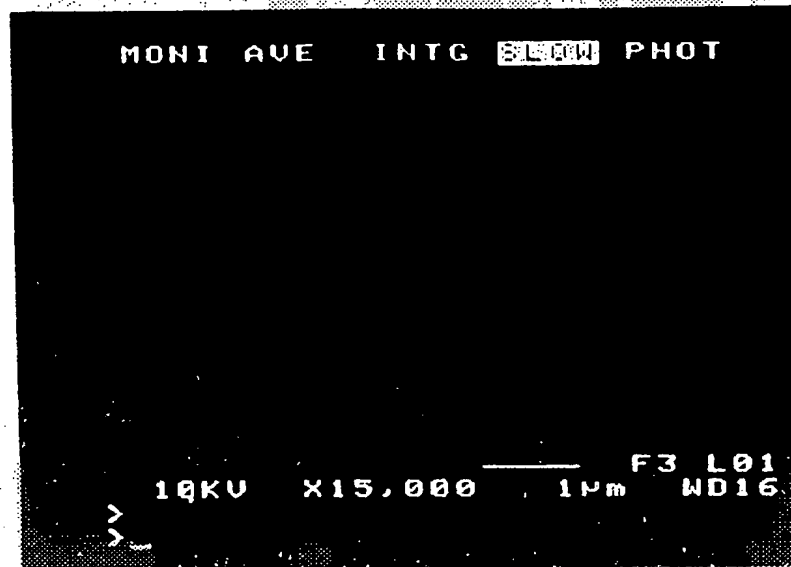
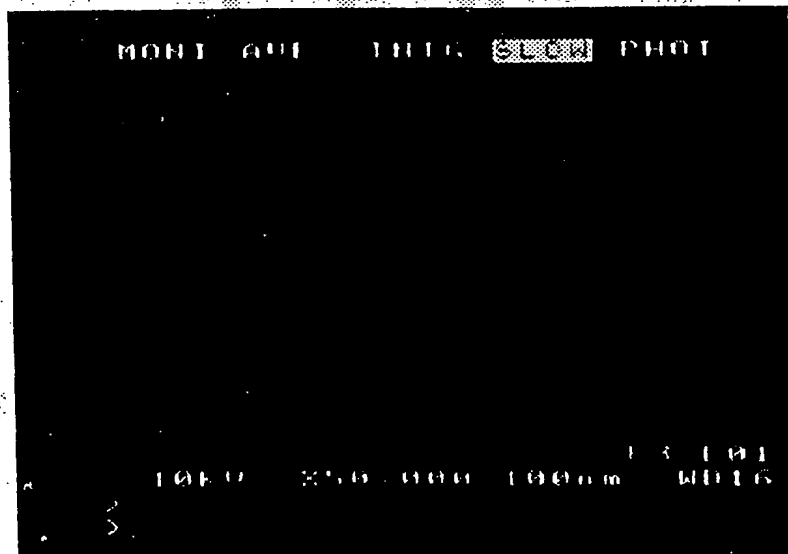
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FIG. 15.



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FIG. 16.FIG. 17.



# INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/21160

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 H01L33/00 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 96 24167 A (ADVANCED TECH MATERIALS ;REDWING JOAN (US); TISCHLER MICHAEL A (US) 8 August 1996 see page 5, line 20 - page 11, line 6 see page 30, line 8 - page 37, line 31	1-7, 12-15
A	---	17-20, 25
Y	WO 90 10950 A (BRITISH TELECOMM) 20 September 1990 see the whole document	1-7, 12-15
A	---	
	PATENT ABSTRACTS OF JAPAN vol. 095, no. 002, 31 March 1995 -& JP 06 326416 A (TOSHIBA CORP), 25 November 1994 see abstract	1, 2, 6-8, 12, 15, 25, 26
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

3 February 1999

Date of mailing of the international search report

10/02/1999

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# INTERNATIONAL SEARCH REPORT

In: International Application No

PCT/US 98/21160

## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>EP 0 352 472 A (TEXAS INSTRUMENTS INC)  31 January 1990  see abstract</p> <p>-----</p>	<p>1,5,17,  19,25</p>



# INTERNATIONAL SEARCH REPORT

Information on patent family members

In: International Application No

PCT/US 98/21160

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9624167 A	08-08-1996	US 5585648 A	17-12-1996
		US 5661074 A	26-08-1997
WO 9010950 A	20-09-1990	CA 2011986 A, C	10-09-1990
		EP 0462995 A	02-01-1992
		JP 4504031 T	16-07-1992
		US 5279687 A	18-01-1994
EP 0352472 A	31-01-1990	JP 2161718 A	21-06-1990
		US 5238869 A	24-08-1993